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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,791	07/02/2004	Yoshifumi Kachi	39.026-AG	6914

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EXAMINER	
CHANDRA, SATISH	

ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/501,791	KACHI ET AL.	
	Examiner	Art Unit	
	Satish Chandra	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-14 are rejected under 35 U.S.C.102 (e) as anticipated by Kuibira et al (US 6,508,884).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Kuibira et al discloses a wafer holder (susceptor) 1 (Fig 5) containing at least one heater 11.

The cross sectional shape 11 (Fig 3) is shown as a rectangular whose lateral and bottom sides perpendicular to each other and having an angle of 90 degrees.

Regarding claims 2, 3, Kuibira et al discloses that the temperature distribution of the wafer in a film deposition process should be within 1% (Column 4, lines 66-67; Column 5, lines 1-2) when the line width and the line interval of the linear pattern of the conductive layer (Column 1, lines 57-60) are each 5 mm or less. And in order to achieve a temperature distribution within 0.5%, the line width and the line interval of the linear pattern of the conductive layer should be 1 mm or less (Column 5, lines 3-4).

Regarding claims 4,8 and 9, Kuibira et al discloses any one of aluminum nitride, aluminum oxide, silicon nitride and aluminum oxynitride (Column 5, lines 15-18) as base material for the wafer holder.

Regarding claims 5 and 10, Kuibira et al discloses the use of aluminum nitride for ceramic substrate having a high thermal conductivity of at least 100 W/m K (Column 5, lines 25-26).

Regarding claims 6, 11, Kuibira et al discloses using at least one metal from the group tungsten, molybdenum, silver, palladium, platinum, nickel or chromium (Column 5, lines 31,32) for forming the conductive layer.

Regarding claim 7, 12-14, Kuibire et al discloses using plasma electrode 12 (Fig 5) as a conductive layer (column 4, lines 5-6).

Claims 1,4,6 are rejected under 35 U.S.C. 102(a) as being as anticipated by Aonuma et al (Patent No. JP02002252269)

Regarding claim 1, Aonuma et al discloses a ceramic susceptor 11 (Fig 2) for processing a wafer wherein the susceptor includes a heating element 12 (Fig 2) embedded therein.

Aonuma et al further discloses that metal electrode (resistive heating element) may be oval, capsular or rectangular and is not limited in its cross sectional shape (Para 0024). This reference teaches resistive heating elements having various cross sectional shapes. When the shape is of a simpler shape such as rectangular, the angle between the lateral and the bottom side is ninety degrees.

Regarding claim 4, Aonuma discloses using an aluminum nitride ceramic substrate (Para 0013, 0019).

Regarding claim 6, Aonuma discloses using one of the metals, either tungsten or molybdenum or platinum or silver in the construction of the metal electrode (resistive heating element) (Para 0023).

Claims 1,4,6 are rejected under 35 U.S.C. 102(b) as anticipated by Hiramatsu et al (Patent No. JP02001244320)

Regarding claim 1, Hiramatsu et al discloses a ceramic susceptor 1 (Fig 3) for processing a wafer wherein the susceptor includes a heating element 5 (Fig 3) embedded therein.

Hiramatsu et al further discloses that metal electrode (resistive heating element) is made in the shape of cusp (Para 0070). This reference teaches resistive heating elements having a pointed shape which could have any angle.

Regarding claim 4, Hiramatsu et al discloses using an aluminum nitride ceramic substrate (Para 0025).

Regarding claim 6, Hiramatsu discloses resistance heating element of either tungsten, molybdenum, nickel material. (Para 0037).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 5, 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aonuma et al (Patent No. JP02002252269) in view of Kuibira et al (Patent No. 6,508,884)

Regarding claims 2, 3, Aonuma et al teach all the limitations of these claims except for achieving a temperature distribution within 1% or 0.5% on the wafer surface.

Kuibira et al discloses that the temperature distribution of the wafer in a film deposition process should be within 1% (Column 4, lines 66-67; Column 5, lines 1-2) when the line width and the line interval of the linear pattern of the

conductive layer (Column 1, lines 57-60) are each 5 mm or less. And in order to achieve a temperature distribution within 0.5%, the line width and the line interval of the linear pattern of the conductive layer should be 1 mm or less (Column 5, lines 3-4).

Therefore it would have been obvious to the person of ordinary skill at the time of invention to provide line width and the line interval of the linear pattern of the conductive layer (Column 1, lines 57-60) of 1 mm or less as taught by Kuibira et al into the apparatus of Aonuma et al in order to achieve temperature distribution within 0.5% or 1.0% (Column 5, lines 1-5).

Regarding claim 5, 10, Aonuma et al discloses using aluminum nitride ceramic with thermal conductivity of 50 or more W/m K.

Aonuma et al does not teach using aluminum nitride ceramic with thermal conductivity of 100 or more W/m K.

Kuibira et al discloses the use of aluminum nitride for ceramic substrate having a high thermal conductivity of at least 100 W/m K (Column 5, lines 25-26)

Therefore it would have been obvious to the person of ordinary skill at the time of invention to use aluminum nitride having a high thermal conductivity of at least 100 W/m k as taught by Kuibira et al into the apparatus of Aonuma et al in order to allow a resultant holder to uniformly heat a semiconductor wafer held thereon (Column 2, lines 64-67).

Regarding claims 8, 9, Aonuma et al discloses using aluminum nitride ceramic substrate (Para 0013, 0019).

Regarding claim 11, Aonuma et al discloses using one of the metals, either tungsten or molybdenum or platinum or silver in the construction of the metal electrode (resistive heating element) (Para 0023).

Regarding claims 7, 12-14, Aonuma et al teaches all the limitations of these claims but does not disclose using plasma electrodes either on the surface or inside the ceramic substrate.

Kuibira et al discloses using plasma electrode 12 (Fig 5) as a conductive layer (column 4, lines 5-6).

Therefore it would have been obvious to the person of ordinary skill at the time of invention to provide a plasma electrode on the surface of or inside a ceramic substrate as taught by Kuibira et al into the apparatus of Aonuma et al in order to generate plasma.

Claims 2, 3, 5, 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramatsu et al (Patent No. JP02001244320) in view of Kuibira et al (Patent No. 6,508,884)

Regarding claims 2, 3, Hiramatsu et al teach all the limitations of these claims except for achieving a temperature distribution within 1% or 0.5% on the wafer surface.

Kuibira et al discloses that the temperature distribution of the wafer in a film deposition process should be within 1% (Column 4, lines 66-67; Column 5, lines 1-2) when the line width and the line interval of the linear pattern of the conductive layer (Column 1, lines 57-60) are each 5 mm or less. And in order to achieve a temperature distribution within 0.5%, the line width and the line interval

of the linear pattern of the conductive layer should be 1 mm or less (Column 5, lines 3-4).

Therefore it would have been obvious to the person of ordinary skill at the time of invention to provide line width and the line interval of the linear pattern of the conductive layer (Column 1, lines 57-60) of 1 mm or less as taught by Kuibira et al into the apparatus of Hiramatsu et al in order to achieve temperature distribution within 0.5% or 1.0%.

Regarding claim 5, 10, Hiramatsu et al discloses using aluminum nitride ceramic with thermal conductivity of 180 W/m K (Para 0025).

Hiramatsu et al does not teach using aluminum nitride ceramic with thermal conductivity between a value of 100 and 180 W/m K.

Kuibira et al discloses the use of aluminum nitride for ceramic substrate having a high thermal conductivity of at least 100 W/m K (Column 5, lines 25-26).

Therefore it would have been obvious to the person of ordinary skill at the time of invention to use either aluminum nitride having a high thermal conductivity as taught by Kuibira et al into the apparatus of Hiramatsu et al in order to allow a resultant holder to uniformly heat a semiconductor wafer held thereon (Column 2, lines 64-67).

Regarding claims 8, 9, Hiramatsu et al discloses using aluminum nitride ceramic substrate (Para 0025).

Regarding claim 11, Hiramatsu et al discloses using one of the metals, either tungsten or molybdenum or platinum or silver in the construction of resistive heating element (Para 0037).

Regarding claims 7, 12-14, Hiramatsu et al teaches all the limitations of these claims but does not disclose using plasma electrodes either on the surface or inside the ceramic substrate.

Kuibira et al discloses using plasma electrode 12 (Fig 5) as a conductive layer (column1, lines 57-60).

Therefore it would have been obvious to the person of ordinary skill at the time of invention to provide a plasma electrode on the surface of or inside a ceramic substrate as taught by Kuibira et al into the apparatus of Hiramatsu et al in order to generate plasma.

Claims 7, 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aonuma et al (Patent No. JP02002252269) in view of Hiiragidaira et al (Patent No. JP2001274103)

Regarding claims 7, 12-14, Aonuma et al teaches all the limitations of these claims but does not disclose using plasma electrodes either on the surface or inside the ceramic substrate.

Hiiragidaira et al discloses using plasma electrode 14 (Fig 6) as a conductive layer either on the surface or inside the ceramic substrate

Therefore it would have been obvious to the person of ordinary skill at the time of invention to provide a plasma electrode on the surface of or inside a ceramic substrate as taught by Hiiragidaira et al into the apparatus of Aonuma et al in order to generate plasma.

Claims 7, 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramatsu et al (Patent No. JP02001244320) in view of Hiiragidaira et al (Patent No. JP2001274103)

Regarding claims 7, 12-14, Hiramatsu et al teaches all the limitations of these claims but does not disclose using plasma electrodes either on the surface or inside the ceramic substrate.

Hiiragidaira et al discloses using plasma electrode 14 (Fig 6) as a conductive layer either on the surface or inside the ceramic substrate

Therefore it would have been obvious to the person of ordinary skill at the time of invention to provide a plasma electrode on the surface of or inside a ceramic substrate as taught by Hiiragidaira et al into the apparatus of Hiramatsu et al in order to generate plasma.

CONCLUSION

Any Inquiry concerning this communication should be directed to Satish Chandra at (571) 272-3769. The examiner can normally be reached on Monday through Friday from 7:00 a.m. to 5:00 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Parviz Hassanzadeh can be reached at 571-272-1435. The fax number for the organization where this application or proceeding is assigned is 703-273-8300

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for the published applications may be obtained from either Private PAIP or Public PAIR. Status information for the unpublished applications is available thorough Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any question (s) on accessing to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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